a plurality of selection circuits respectively associated with said plurality of memory arrays, selectively and independently disabling said first memory block and selecting said second memory block, when said first memory block is defective and said second memory block is normal.

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67. A semiconductor memory as claimed in claim 66, wherein said selection circuit disables said defective, first memory block and selects said normal, second memory block in accordance with specific signals.--

REMARKS

By this Preliminary Amendment, the original parent application claims are being canceled, and new claims 63-67 are being substituted therefor. These new claims are exact copies of claims 1, 4, 6, 10 and 14, respectively, of patent no. 5,668,763 of Fujioka et al., issued September 16, 1997.

The Specification is also being amended to substitute a new title that is more descriptive of the claimed subject matter, to cross-reference parent applications, and to update the status and patent numbers for applications referenced in the text. Since the referenced application serial no. 204,175 has issued as patent no. 5,095,344, the patent number is being added by this Amendment. The serial number of the second referenced application is also being added by this Amendment. The status of the second referenced application is that it has become abandoned in favor of a continuation-in-part application which matured into patent no. 5,172,338 and a division thereof into patent no. 5,163,021.

An early examination and allowance of the present application are solicited.

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Respectfully submitted,

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